Barrier roughness effects in resonant interband tunnel diodes

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Peak current densities of InAs/AlSb/GaSb/AlSb/InAs resonant interband tunneling diodes (RITD) grown by molecular beam epitaxy have been measured as a function of the growth temperature. The growth procedures were designed to produce nominally identical AlSb tunneling barriers. The variations observed in the peak current for positive bias are consistent with the barrier on the substrate side of the RITD becoming effectively thicker for diodes grown at high temperatures. Plan-view *in situ* scanning tunneling microscopy (STM) measurements indicate that smoother AlSb barriers are grown at high temperature. The growth temperature dependence of the peak current density and STM results are consistent, because tunneling is highly dependent on barrier thickness. While the high and low temperature growths were designed to have the same barrier thickness, the large current flowing through the thin areas of a rough barrier result in an effectively thinner barrier compared to the smooth one. © *2001 American Institute of Physics.* [DOI: 10.1063/1.1415539]

I. INTRODUCTION

Interface roughness has often been discussed as a factor in determining the current through resonant tunneling diodes that are of interest for use in high-speed electronic devices. Monolayer (ML) fluctuations in tunnel barrier thickness are expected to be important, because it is necessary to use tunnel barriers only a few ML thick to obtain the high peak current densities required for high-speed devices. There have been many theoretical discussions on the importance of surface roughness and the interface scattering mechanisms that contribute to peak and valley currents in (Ga,In)As/AlGaAs resonant tunneling devices.[1–11] On the experimental side in the (Ga,In)As/AlGaAs material system, there have been reports aimed at linking barrier roughness measured by scanning tunneling microscopy (STM), or a spectroscopic method such as photoluminescence, to device performance.[12–16] Currently, there is little information available for the interband tunneling devices that use the 6.1 Å lattice constant materials, InAs/AlSb/GaSb, and are currently under development for applications in high-speed, low power electronics.[17–20] The low-power possibilities arise because the negative resistance peak in this material system occurs near 100 meV. RITDs also exhibit high peak current densities near 10^5 A/cm^2 that are desirable for high-speed applications, and large peak-to-valley current ratios (P/V) that help minimize power dissipation.

The roughness phenomenon of interest here is the variation in tunneling barrier thickness on a monolayer scale. Although the growth procedures are designed to produce AlSb barriers of a uniform thickness, the mechanics of the growth may result in the redistribution of the AlSb with some areas that are thicker and some that are thinner than planned. Because the tunneling probability increases exponentially with decreasing barrier thickness, the thinner parts of a barrier will carry more current than expected based on the design and the thicker parts will carry less. The net result would be a higher current than expected, with the barrier appearing thinner than anticipated based on the growth parameters. Barrier roughness features with dimensions on the order of the Fermi wavelength may also cause interface scattering. Such scattering events may transfer electrons from states with a low probability of tunneling to states with a higher tunneling probability, thereby also increasing the tunneling current.

The properties of a barrier may also be affected by intermixing caused by the exchange or segregation of the barrier atoms with those of the well or electrodes. Segregation or exchange of Ga or In from the well or electrode would create an AlGaSb or AlInSb alloy barrier with a narrower band gap than AlSb, and larger current densities than expected. In contrast, the incorporation of As would create an AlAsSb barrier with a wider band gap and lower current densities. The possibilities of these events occurring are discussed below.

Interband resonant tunneling can be understood by considering the RITD layer structure and the corresponding energy bands pictured in Figs. 1(a) and 1(b). As shown here, a RITD consists of a pair of wide-band-gap AlSb tunnel barriers, and a GaSb well sandwiched between *n*-type InAs electrodes. An electron in the conduction band (CB) of an InAs electrode tunnels through the band gap of an AlSb barrier into the valence band (VB) of the GaSb well, through the second AlSb barrier into the CB of the other InAs electrode. This band structure results in high peak current densities and large peak-to-valley current ratios at room temperature. It also leads to a complicated set of boundary conditions as the conduction band electrons tunnel via both light and heavy hole valence band levels in the GaSb well. Details of the band mixing in the GaSb well and the role of interface phenomena are open questions.

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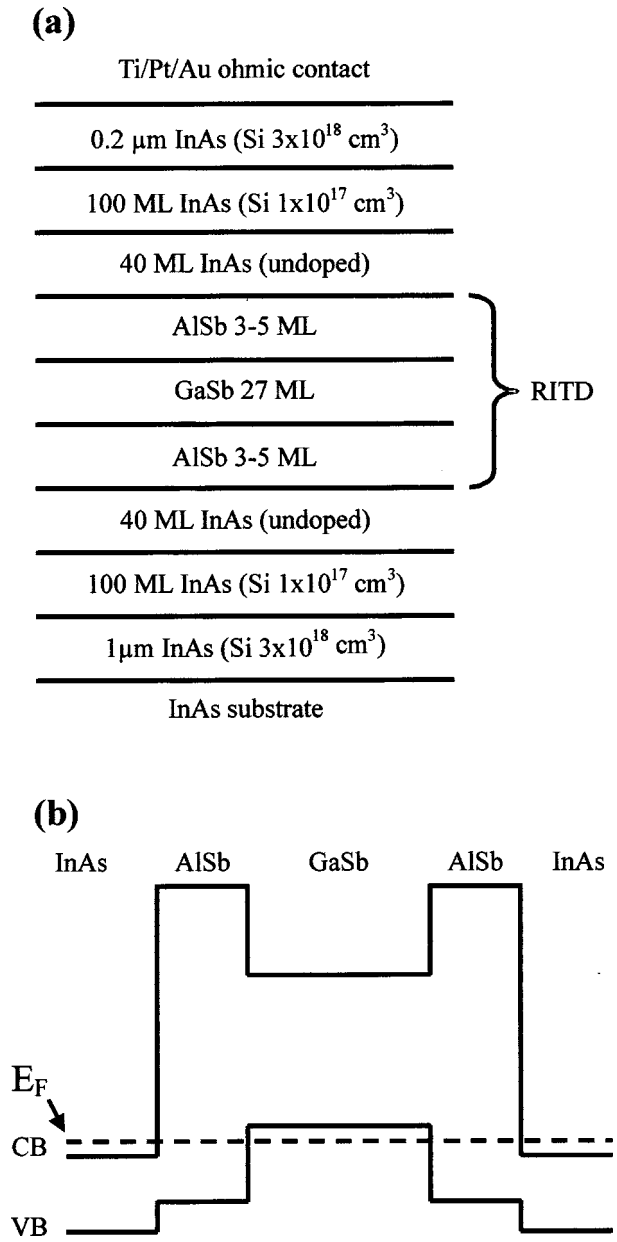

FIG. 1. (a) Layer structure for a RITD, (b) and the band edge diagram.

II. EXPERIMENT

The diodes examined here were grown by molecular beam epitaxy (MBE) on InAs (001) substrates. As illustrated in Fig. 1(a), the growth starts with a buffer layer consisting of 1 μm $n+$ InAs followed by 100 ML of n^- InAs and then 40 ML of undoped InAs. The RITD structure consists of a pair of nominally identical AlSb barriers sandwiching a 27 ML GaSb well. It is covered with 40 ML of undoped InAs, then 100 ML n^- InAs and finally 0.2 μm of n^+ InAs. Migration-enhanced epitaxy growth procedures similar to those described in Ref. 21 were used to form InSb interfacial bonds at the InAs/AlSb interfaces. The interface for the bottom barrier was formed by depositing 1 ML of In on an As-terminated InAs surface followed by several seconds of exposure to Sb_2. A valved cracking cell was used as the arsenic source, and the valve was closed during the AlSb and GaSb growths to minimize As incorporation in these layers. Reflection high-energy electron diffraction (RHEED) measurements were used to calibrated growth rates. The substrate temperature during growth was monitored by a thermocouple, calibrated by observing the InAs $(2\times4)\rightarrow(4\times2)$ transition in the absence of an arsenic flux (460 °C). Two sets of samples, one with 3 ML thick AlSb barriers and the other with 5 ML barriers, were grown with substrate temperatures between 350 and 500 °C. Standard photolithography techniques were used to pattern Ti/Pt/Au ohmic contacts with diameters ranging from 2 to 50 μm. Mesas were formed by using the ohmic contacts as the etch stop in a wet etching process. Current–voltage ($I-V$) measurements were made at room temperature by tensioning a fine gold wire point contact against the ohmic contact on a mesa [the large area back contact is not illustrated in Fig. 1(a)]. In the data plots, "positive bias" means the top of the mesa is biased positively with respect to the substrate. The data represent average values for several mesas measured on a chip. A third set of samples was grown for plan-view STM measurements. Some of these samples were used to study the homoepitaxial growth of InAs, with the goal of developing procedures for obtaining smooth InAs surfaces as the first step in the growth of resonant tunneling devices.[21] Other samples were grown to examine the growth of AlSb on InAs to determine the factors required to obtain smooth barriers for resonant tunnel diodes. Detailed reports of these and related STM studies by others have already been published,[21–27] and notably, the growth temperature has been found to be a contributing factor in obtaining smooth AlSb barriers. This report examines the correlation of the growth temperature changes observed by STM and $I-V$ measurements. Although peak and valley currents are presented for both bias polarities, this article focuses on the temperature dependent changes observed when a positive bias is applied. Data are presented to demonstrate that changes in the bottom barrier result in relatively large changes in the positive bias peak current, and have little effect on the negative bias currents.

III. RESULTS

The peak and valley currents for both positive (I_{p+},I_{v+}) and negative (I_{p-},I_{v-}) bias were measured in the course of this work. Theory predicts $I_{p+}=I_{p-}$ and $I_{v+}=I_{v-}$ for identical barriers, but experimental measurements often exhibit asymmetries. Even if an AlSb layer is grown on a smooth InAs surface, the AlSb may have ML scale variations in its thickness depending on whether the growth proceeds by step flow or by the nucleation and growth of islands. The way that an asymmetry in a RITD due to different barrier thickness would be manifest in $I-V$ data is illustrated in Fig. 2, where data for a device with nominally identical top and barriers are plotted along with data for a deliberately asymmetric one. Similar peak current densities, for both positive and negative bias, are found in Fig. 2 for the diode with 5 ML top and bottom barriers. This is in contrast to the asymmetric $I-V$ obtained for the diode with an 8 ML bottom barrier and a 5 ML top barrier. The positive bias peak current for the diode with an 8 ML bottom barrier is much smaller than the positive bias peak current for the diode with a 5 ML

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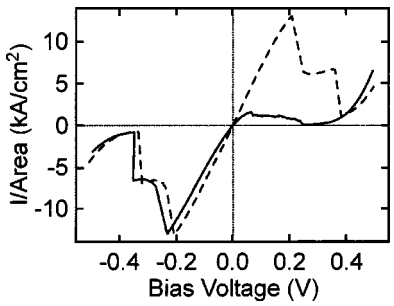

FIG. 2. Comparison of $I-V$ curves for a RITD with nominally identical 5 ML thick AlSb barriers (dashed lines) with an asymmetric RITD with an 8 ML bottom barrier and a 5 ML top barrier (solid line).

bottom barrier. Very similar negative bias peak currents are found for the two diodes. These comparisons demonstrate that variations in the thickness of the bottom barrier result primarily in differences in the positive bias peak current. The voltages where the current peaks occur also differ for the two devices with similar voltages ($V_{p+} \approx V_{p-}$) for the symmetric device, while V_{p+} is very different from V_{p-} for the asymmetric diode. These voltage differences will not be discussed here, as they are in part due to series resistance effects, as well as to the accumulation of charge in the well.

STM studies of the growth of AlSb on InAs indicate that the substrate temperature is an important factor in the morphology of the AlSb layer.[21] Hence, we have examined the dependence of the $I-V$ characteristics on growth temperature in search of evidence of barrier roughness phenomena. The data presented in Fig. 2 indicate that changes to the bottom AlSb barrier, which is grown on InAs, will be reflected in the positive bias peak current density. Thus, the focus of this article will be on the changes in the positive bias data with increasing growth temperature. The peak and valley current densities for a series of samples with nominally identical 3 ML thick barriers grown with substrate temperatures between 350 and 500 °C are presented in Fig. 3. The positive bias peak current decreases significantly on increasing the growth temperature, while there is a slight increase in the negative bias peak current. A similar decrease in the positive bias peak current is illustrated in Fig. 4(a) for a series of samples with 5 ML thick barriers. The behavior of the positive bias peak current for both sets of diodes is consistent with an increase in the effective thickness of the bottom AlSb barrier with increasing growth temperature. The larger decrease in the peak current density for the 3 ML samples compared to the 5 ML set is also consistent because diodes with 5 ML barriers should be less sensitive to ML-scale thickness fluctuations than those with 3 ML barriers.

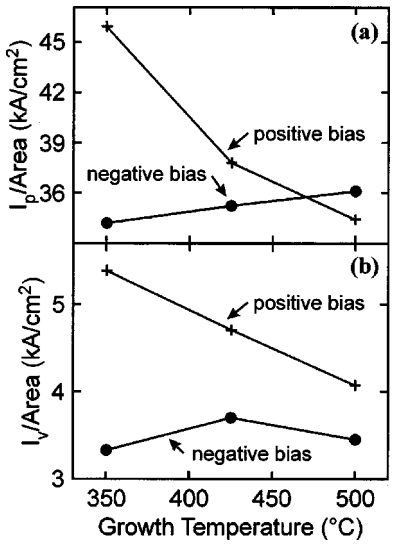

FIG. 3. Dependence of the current density on the growth temperature for RITDs with 3 ML AlSb barriers: (a) peak current and (b) valley current.

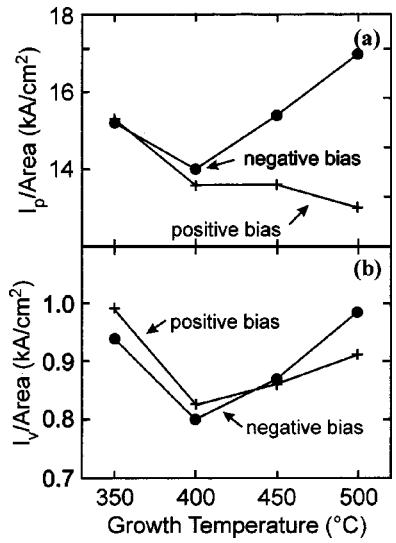

FIG. 4. Dependence of the current density on the growth temperature for RITDs with 5 ML AlSb barriers: (a) peak current, and (b) valley current.

The dependence of the valley currents on the growth temperature is more complex than the behavior of the peak currents. The positive bias valley current in Fig. 3(b) decreases, as does the peak current, suggesting that the effective barrier thickness may be a dominant factor for I_{v+} for these diodes. A different behavior is found in Fig. 4(b) for the diodes with 5 ML barriers. For these diodes, the positive bias valley current increases, while the peak current decreases for all but the sample grown at 350 °C.

The topography of 5 ML thick AlSb layers grown on InAs obtained by *in situ* STM is illustrated in Fig. 5(a) for a growth temperature of 400 °C and in Fig. 5(b) for 470 °C. Note that a slightly different procedure was used to prepare the interfaces between these AlSb layers and the InAs than was used for the RITDs in Figs. 3 and 4. In Fig. 5, the interfaces were formed by depositing 1 $\frac{1}{4}$ ML of In vs 1 ML used for the RITD samples. The details of the difference are discussed in Ref. 21, where it is shown that the extra $\frac{1}{4}$ ML of In results in a slightly smoother InSb interfacial bond layer. The different gray scales in Fig. 5 delineate topographic heights varying by a single AlSb layer (i.e., 1 ML or 0.3 nm), with the darker levels therefore corresponding to locally thinner regions of the AlSb than the brighter levels. A comparison of the relative areas covered by the different thicknesses on a given terrace reveals that the 400 °C growth the low to high regions occupy 21%, 67%, and 11% of the area compared to 3% for the low and 17% for the highest areas of

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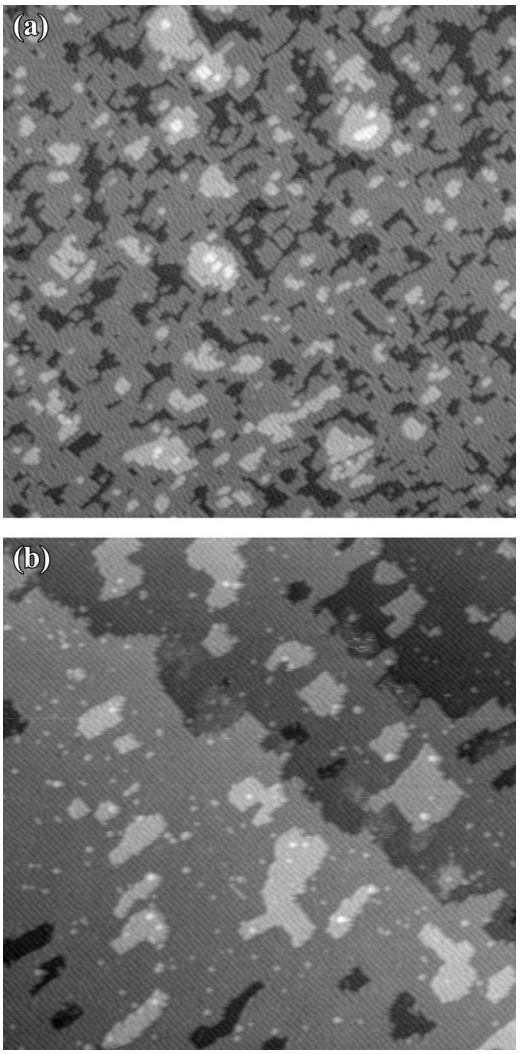

FIG. 5. Plan-view STM images, 130 nm×130 nm, of 5 ML thick AlSb layers grown on InAs at (a) 400 °C, and (b) 470 °C.

the 470 °C sample. As thin areas cover a larger portion of the 400 °C sample than they cover for the 470 °C one, the effective barrier thickness for the low temperature growth is less than for a high temperature growth . This result is consistent with the $I-V$ data for both the 3 and 5 ML barriers, where a higher current through the bottom barrier is found for the lower temperature growths.

It is difficult to attribute the decrease in current density with increasing growth temperature to an alloying affect of the lower barrier. Indium segregation into AlSb from InAs has been suggested as an explanation for defect related features in a cross-sectional STM (XSTM) study of infrared laser structures, indicating the bottom AlSb barrier might contain In.[27] However, an InAlSb barrier would have a smaller band gap than AlSb causing a higher current density than an AlSb barrier.[28] Moreover, because In segregation is an activated process, the In concentration would be expected to increase with growth temperature, causing an increase in current with growth temperature contrary to our results. Although some In may be present in the barriers used here, its presence is clearly not the dominant factor in the growth temperature dependence of the current.

A decrease in the current due to an alloying effect would be expected from an AlAsSb barrier. However, the concentration of As in these barriers is believed to be very low. A related XSTM study of laser structures grown with similar procedures did not observe As in AlSb layers grown on InAs.[27] In addition, our use of InSb interfacial bonds is believed to prevent segregation of As into the lower AlSb barrier from the adjacent InAs layer. Finally, we closed the valve to the As cracker during AlSb growths, a procedure shown to minimize As cross incorporation.[22]

To understand the role of the morphology of the InAs/AlSb interface, RITDs were prepared using either 1 $\frac{1}{4}$ or 1 ML of In in the formation of the InSb interface bonds for the bottom carrier.[21] The STM images in Fig. 5 indicate that relatively smooth AlSb barriers are obtained at the growth temperature of 470 °C. The negative bias peak currents for the 1 $\frac{1}{4}$ and 1 ML In are very similar at 24 and 25 kA/cm^2, respectively. Different positive bias peak currents were measured, with the 1 $\frac{1}{4}$ ML In diode having a current of 19 kA/cm^2 compared to 23 kA/cm^2 for the 1 ML diode. This is consistent with having a slightly thicker bottom AlSb barrier associated with a more uniform barrier thickness achieved with the modified interfacial layer.

IV. SUMMARY

The role of barrier roughness in the $I-V$ characteristics of resonant interband tunnel diodes has been examined by comparing the peak current densities with plan-view STM topographies of AlSb layers grown at similar substrate temperatures. RITDs grown at high temperatures have been found to have smaller positive bias peak currents than those grown at lower temperatures. This indicates that the high temperature growths result in an effectively thicker bottom barrier than growths at low temperatures even though the growths were designed to produce barriers with the same thickness. The effective thicknesses differ from the planned thickness because the thinner regions produce a current increase that is proportionally larger than the current decrease in the thicker regions. The amount of roughness affects the relative portion of the area covered by thin barriers compared to thick barriers. $I-V$ measurements were done on one set of samples with 3 ML barriers and on a second set with 5 ML barriers, and the positive bias peak currents behaved similarly as a function of growth temperature. A smaller decrease in the positive bias peak current is found for diodes with 5 ML barriers than for those with 3 ML barriers, as expected, because roughness should have a larger impact on the thinner barriers. STM images of AlSb layers grown on similarly prepared InAs over a similar temperature range demonstrate that AlSb layers grown at low temperatures have more areas covered by relatively thin regions than those grown at higher temperatures. Therefore, we conclude that changes in the barrier topography, not barrier composition, caused the current density decrease with increasing growth temperature.

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