

Metamorphic AlSb/InAs HEMT for Low-Power, High-Speed Electronics

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I. ABSTRACT

Metamorphic high electron mobility transistors (HEMT) on GaAs substrates, with InAs channels and 0.1- μm metal gates, have demonstrated 5 to 10 times lower power dissipation for equivalent f_T over conventional InAlAs/InGaAs lattice-matched HEMT's and MHEMT's. Our AlSb/InAs HEMT's exhibit transconductances higher than 1S/mm at drain biases as low as 0.2 V, while maintaining measured f_T results greater than 200 GHz and f_{MAX} results approaching 200 GHz. We have achieved low power X-band MMIC low-noise amplifiers with greater than 7 dB/stage peak gain from 12-14 GHz and 6 mW/stage DC power dissipation.

II. INTRODUCTION

Monolithic Millimeter-wave Integrated Circuits (MMIC) based upon InAs-channel HEMT's have the potential to enable revolutionary low-noise, low-power, and high-speed applications. InAs electronic properties, such as electron mobility and peak velocity, are nearly two times larger as compared to state-of-the-art $\text{In}_x\text{Ga}_{1-x}\text{As}$ -channels.

InAlAs/InGaAs HEMT's grown on lattice-matched InP substrates offer the best combination of low-power and low-noise MMIC's to date [1-2]. Based on our device data, as shown in Figure 1, we estimate InAs-based HEMT performance meets or exceeds InAlAs/InGaAs HEMT's but with only one-tenth the power dissipation.

However, lattice-matched growth of InAs-channel HEMT is not pragmatic due to a lack of viable 6.05 \AA substrates. Researchers have utilized thin InAs layer inserts within InGaAs channels to achieve marked improvements in electron quantum well transport [3]. However the width of the compressively strained InAs typically does not exceed 50 \AA due to the critical thickness limits on a 5.9 \AA lattice.

Metamorphic growth using the $\text{Al}_x\text{Ga}_{1-x}\text{Sb}_y\text{As}_{1-y}/\text{InAs}$ material system, which has a lattice constant near 6.1 \AA , has proven to be a viable alternative for state-of-the-art InAs-channel HEMT's [4-7]. Researchers in this field now routinely achieve electron mobility $> 15,000 \text{ cm}^2/\text{V}\cdot\text{s}$ with

tensile strained InAs channels. However, the approach does hold several unique challenges such as intrinsic material stability, gate leakage, and yield limiting defect densities, which have been incrementally addressed over the years [7]. Only recently has the first AlSb/InAs HEMT-based MMIC been demonstrated [8].

○ InAlAs/InGaAs HEMT & MHEMT: 75 mW/mm
● AISb/InAs HEMT: 6 mW/mm

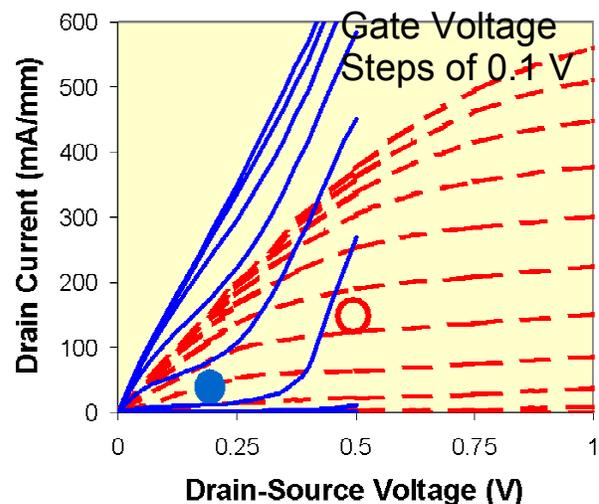


Figure 1. AISb/InAs HEMT (solid) bias points for minimum noise figure and lowest DC power dissipation, compared to InAlAs/InGaAs HEMT (dashed). Curves displayed for gate voltage step of 0.1 V.

In this paper, we will discuss the successful development of a manufacturable AISb/InAs HEMT technology at Northrop Grumman Space Technology (NGST) and Naval Research Laboratory (NRL) for ultra low-power, high-frequency MMIC products.

This technology holds particular promise for application in large area, millimeter-wave phased-array receiver systems. Radically reduced electrical power dissipation per

element greatly benefits these systems due to cumulative savings in energy consumption. The savings can translate to an order of magnitude reduction in combined size/weight of power supplies, distribution network, and thermo-mechanical packaging, or conversely to an order of magnitude larger array area for enhanced sensor resolution. In either case, this technology may enable smaller, lighter phased array solutions that are cheaper to manufacture and maintain.

III. DEVICE GROWTH AND FABRICATION

A. Growth and Profile Design

The AlSb/InAs structures were grown by molecular beam epitaxy (MBE) on semi-insulating 3" and 2" GaAs substrates. Whereas NRL utilizes both substrate sizes, NGST grows strictly on 3" substrates to utilize flight-qualified processes within our GaAs & InP frontside production lines. Both labs have grown several wafers of a standard structure, as shown in Figure 2, to qualify the transference of growth and frontside process methodology, as well as comparative analysis.

Layer	Device	Thick. (Å)	Doping
	LOW-NOISE		
Cap	InAs	20	
Hole Barrier	In _{0.40} Al _{0.60} As	40	
Electron Barrier	AlSb	12	
Doping	InAs-Si	12	3e19 (Si)
Electron Barrier	AlSb	75	
Channel	InAs	150	
Back Barrier	AlSb	500	
Buffer Cap	Al _{0.70} Ga _{0.30} Sb	3000	
Relaxed M.M. Buffer	AlSb	17000	
GaAs Buffer	GaAs	2300	
Substrate	GaAs	-----	S. I.

Figure 2. Layer structure of one standard profile grown at NGST and NRL.

Both labs schedule destructive Hall measurements of as-grown standard profile wafers and perform non-destructive sheet resistance mapping on every grown wafer for statistical process control monitoring (SPCM). According to SPCM statistics, the standard profile grown by NGST obtains an average sheet resistance of 180.5 Ω/sq with less than 2.6% non-uniformity and 300K mobility of 19,100 cm²/V*s with electron sheet density of 1.77x10¹² cm⁻². Also, SPCM confirms that NRL grown equivalent profiles have similar characteristics: average sheet resistance of 172 Ω/sq with less than 3.5% non-uniformity. The fact that state-of-the-art growth of Al_xGa_{1-x}Sb_yAs_{1-y}/InAs HEMT profiles can be successfully controlled in both research and

pre-production MBE reactors is a testament to its reproducibility. Detailed technical rationale regarding the implementation of the hole barrier, modulation doping, and buffer cap in our standard profile can be found in previous publications [4,5,9].

We have also fabricated HEMT's on similar heterostructures using Te modulation doping and other Si doped profiles. In both cases, sheet resistances less than 100 ohms/sq have been achieved. These device results will be reported elsewhere. However, we expect that reduced sheet resistance through improved mobility may be possible even for our standard profile. An NRL grown Hall sample has demonstrated 300K mobility of 29,300 cm²/V*s with sheet density of 1.27x10¹² cm⁻². To date, this stands as the highest mobility result that either lab has achieved with the standard profile.

B. Fabrication

The NGST device fabrication process has centered on achieving MMIC production compatibility. Therefore, there are significant differences between NGST and NRL baseline fabrication processes. For the device, these center upon the mesa isolation step and sequence, E-beam lithography, gate metallization, nitride passivation, and use of qualified InP-HEMT production optical-stepper lithography, cleaning procedures, SPCM testing, and database tracking.

Active device mesas were formed by using a BCl₃/Ar-based Inductively-coupled Plasma (ICP) etch to remove 1250 Å of the structure. The mesa isolation process was designed to end in the Al_{0.7}Ga_{0.3}Sb layer, and achieves an average of 100 MΩ/sq of electrical isolation resistance without the need for implant isolation. This level of isolation is comparable to NGST's space-qualified, production InAlAs/InGaAs/InP HEMT's that employ both mesa isolation and implant isolation. Pd/Pt/Au ohmics alloyed at 175°C in a nitrogen atmosphere formed contacts with a resistance of 0.06 Ω*mm.

Electron beam lithography was utilized to fabricate 0.1 μm Mo/Au T-gates in a 2 μm source-drain region. The source to gate distance was 0.8 μm. A tilted-view SEM of a completed device is shown in Figure 3, which shows the shallow step of the 0.1 μm gate length T-gate down to the AlGaSb mesa floor.

Our MMIC integration process is identical to our flight-qualified InAlAs/InGaAs/InP HEMT process [10]. This process features devices and passive circuit components which are fully passivated with a total of 750 Å PECVD SiN, two levels of interconnect metal including airbridges, 300 pF/mm² double-layer MIM capacitors with breakdown voltages over 100 volts, and 100-Ω/sq precision NiCr resistors with 0.6 mA/μm reliable operation.

Upon completion of frontside processing, wafers were thinned to a thickness of 50 μm. Round 25 μm diameter vias were etched through the substrate to allow contact from the HEMT source pads to the backside wafer ground plane.

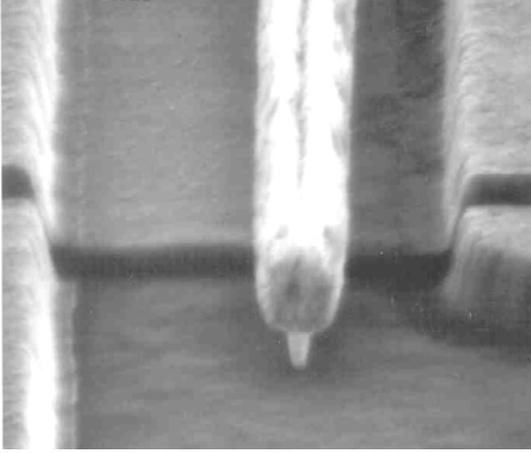


Figure 3. Scanning electron microscope photo showing a tilted-view of 0.1- μm T-gate over shallow ICP-etched mesa isolation step.

IV. RESULTS

Devices were DC tested on-wafer at the completion of processing. The devices displayed high transconductance (G_M) at low drain-source voltage (V_{DS}), and low on-state resistance (R_{ON}). The average G_M peak was 1.05 S/mm and 2.56 S/mm measured at a V_{DS} of 0.2 V and 0.4 V respectively. The average off-state reverse gate-drain breakdown (BV_{GDR}) was -1.42 V (measured at a gate current of -1 mA/mm). An example of the DC drain current (I_D) versus V_{DS} is shown in the top of Figure 4, while G_M vs. gate voltage (V_G) is shown in the bottom. DC characteristics in Figure 4 were measured from a 2-fingered 80- μm total gate periphery device with typical extrinsic R_{ON} of $0.67 \Omega^*\text{mm}$. These characteristics illustrate the combination of low drain voltage operation, low knee voltage, and high transconductance, which are critical parameters for ultra-low power, high frequency operation.

Although DC G_M demonstrates levels > 2 S/mm for $V_{DS} > 0.4$ V, unity current gain frequency (f_T) doesn't increase proportionately with DC $G_M > 0.3$ V V_{DS} , as shown in the bottom of Figure 4. This effect is attributed to the significant shifts in the static gate-channel potential that can occur with impact ionization current and is characterized by a marked bell-shaped dependence in the gate current (I_G) vs. V_G characteristic shown in Figure 5, starting at $V_{DS} > 0.3$ V.

Small signal RF tests were also performed on-wafer, and the average peak f_T was 153 GHz and 212 GHz at V_{DS} of 0.2 and 0.4 volts and drain current densities of 115 and 340 mA/mm, respectively. These correspond to DC power dissipations of 22 and 180 mW/mm. Compared to f_T -DC power performance of state-of-the-art 0.1- μm gate length InAlAs/InGaAs/InP HEMT's, our AlSb/InAs HEMT's provide equivalent high-speed figure of merit performance at 5 to 10 times lower power dissipation, as shown in Figure 6.

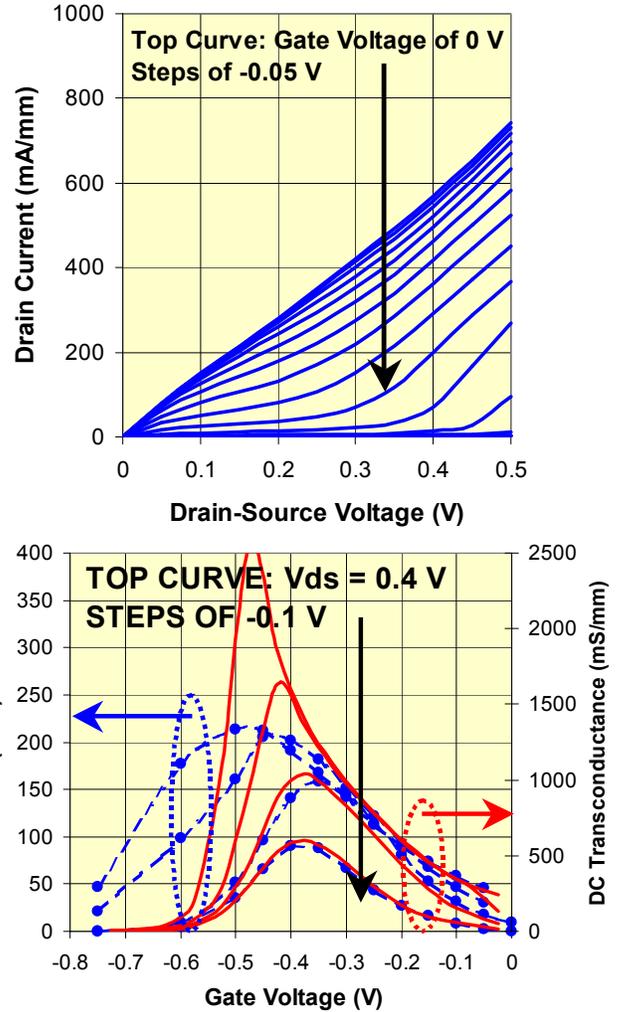


Figure 4. Top: Measured drain current vs. drain voltage and Bottom: Extrapolated unity current gain frequency (dashed) and measured DC transconductance (solid) vs. gate voltage.

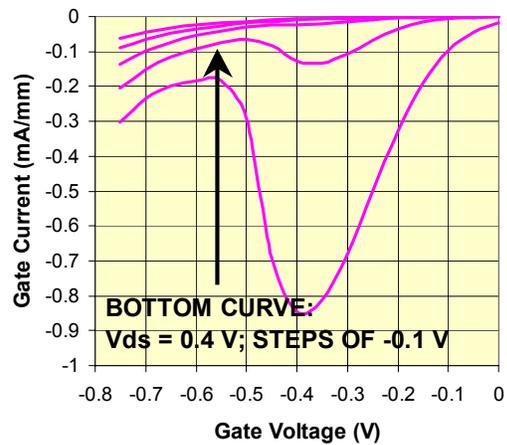


Figure 5. Measured gate current vs. gate voltage.

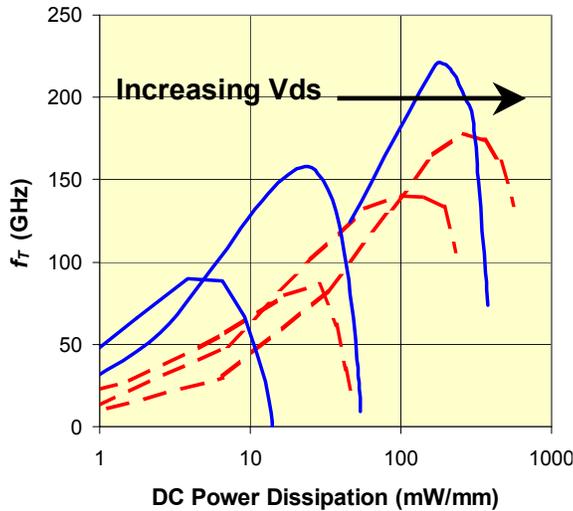


Figure 6. Extrapolated unity current gain frequency vs. DC power dissipation for AlSb/InAs HEMT (solid) at $V_{DS} = 0.1, 0.2,$ and 0.5 volts and InAlAs/InGaAs HEMT (dashed) at $V_{DS} = 0.2, 0.5,$ and 1.0 volts.

Measured small-signal characteristics, shown in Figure 7, of a 1-stage balanced MMIC LNA cell has demonstrated unconditional stability from 50 MHz to 50 GHz, and 12 to 14 GHz gain > 7 dB with > 10 dB input and output return loss matching at a DC power dissipation of only 6 mW. This is the highest gain, lowest power dissipation per stage X-band amplifier performance that we know of to date.

MMIC's reported here were achieved with a tellurium-doped variation of our standard profile, grown by NRL, and NGST's nominally $0.15\text{-}\mu\text{m}$ gate length AlSb/InAs HEMT process. We expect even better gain vs. DC power dissipation from MMIC's achieved with our baseline profile and $0.1\text{-}\mu\text{m}$ gate length process due in part to substantially better f_T -low DC power characteristics as reported here, and f_{MAX} performance approaching 200 GHz, which is one of the highest such performances reported for AlSb/InAs HEMT's to date.

V. CONCLUSION

NGST and NRL have demonstrated a high performance and highly reproducible AlSb/InAs HEMT technology. The combination of ultra-low power dissipation and excellent high-frequency performance will enable revolutionary reductions in size, weight, and cost of millimeter-wave phased-array receiver systems.

VI. ACKNOWLEDGEMENTS

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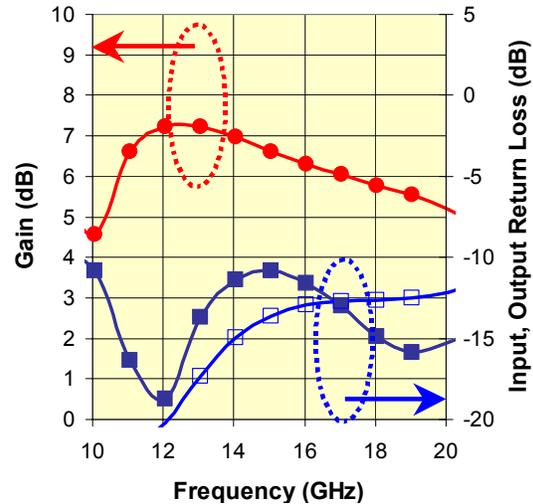


Figure 7. Measured gain (solid circles), input (solid rectangles) and output (open rectangles) return loss of a 1-stage balanced X-band MMIC LNA.

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