



Magneto-electronic latching Boolean gate

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Received 20 September 1999; accepted 2 November 1999

Abstract

We present a magneto-electronic device family with the unique characteristic that the “family” is composed of a single device that can perform any of several Boolean functions, with the function dynamically determined *during the operation* by the manner in which the device is addressed. As the device operates in a latching mode, it also performs a nonvolatile storage function. Integration of logic and memory is achieved, so that memory and processing functions can be dynamically apportioned. © 2000 Elsevier Science Ltd. All rights reserved.

Keywords: Magneto-electronics; Nonvolatile memory; Programmable logic; Hall effect; Boolean gate; InAs

Nomenclature

H	magnetic field, Oe
H_c	magnetic coercivity, Oe
M	magnetization, G
B_z	magnetic field in the z direction, Oe
I	current, A
V_H	Hall voltage, V
H_x	magnetic field in the x direction, Oe
f	feature size, nm
ΔR_H	change in Hall coefficient, Ω
R'	series resistance, Ω
α	inductive constant, Oe/A
R_{\square}	sheet resistance, Ω/\square

1. Introduction

In the dominant transistor based logic families, complementary metal-oxide-silicon (CMOS) and transistor-transistor logic (TTL), a single Boolean gate is

“hard wired” in the form of a particular combination of several field effect transistors (FETs) or bipolar transistors. By contrast, a single resonant tunneling diode (RTD) can be used as an exclusive OR (XOR) gate (see e.g. Ref. [1]) and thereby shows promise for faster gate operation and increased packing density. A single device that could perform multiple Boolean operations would offer greater utility and even higher densities.

Applications of *magneto-electronic* devices (electronic devices that incorporate a ferromagnetic component) have included analog sensors [2] and digital storage cells [3–5], utilizing the sensitivity to magnetic fields and the nonvolatility of the bistable, hysteretic state of a ferromagnetic element, respectively. However, other properties of magnetism can also be exploited: The functional form of the magnetization $M(H)$ of an ideal microstructured ferromagnetic element is symmetric about zero magnetic field, $H = 0$, is multivalued for fields H smaller than the coercivity, $|H| < |H_c|$, and has a zero slope for larger fields, $|H| > |H_c|$. Using these properties, we introduce a magneto-electronic logic family that offers unprecedented flexibility. It permits logic operations to be continuously programmed and reprogrammed at the most basic, cellular level, that of a single Boolean process, and on the time scale of a *single clock cycle*. As our prototype devices also demonstrate a nonvolatile memory function, large-scale integration of logic and memory on the same chip is automatically achieved and,

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further, memory and processing can be dynamically and continuously apporportioned.

2. Sample preparation and experimental procedure

Magneto-electronic devices are well suited to digital applications because of the intrinsic bistability of ferromagnetic films. To perform digital logic, a device with appropriate binary input and output characteristics is needed. The bistable magnetic states must correlate with logical LOW and HIGH (binary “0” and “1”) electronic states, i.e. the levels of transmitted voltage or current pulses.

Appropriate output characteristics are provided by the ferromagnet–semiconductor nonvolatile gate (also called the *hybrid Hall effect device*) [6–9], a bilayer structure composed of a semiconductor channel and a single, electrically isolated, ferromagnetic element. An atomic force microscope (AFM) image of a prototype device is shown in Fig. 1A. In this false color image, the ferromagnetic element F is red, the mesa structure of a high mobility InAs/GaAlSb heterostructure is brown, and ion-damaged regions that are electrically insulating (described below) are green. As seen in the cross-section view (Fig. 1C), F is fabricated on insulator I_1 and is electrically isolated from the carriers in the InAs single quantum well (SQW, purple) which is grown on insulating buffer layer I_2 . The bistable, in-plane magnetization \vec{M} of F can be oriented to the left or right ($\mp\hat{x}$) corresponding to the binary values “1” and “0”, respectively. The magnetic film F functions as a source of locally strong magnetic fields that act on the carriers in the SQW. When \vec{M} is oriented to the left as in Fig. 1C, there is a region of field with a large component $-B_z$ directly under the edge of F ,¹ and a Lorentz force on a positive bias current I results in a positive Hall voltage V_H sensed in the transverse arms of the cross (Fig. 1A). When \vec{M} is reversed and points to the right, the local field changes sign and the Lorentz force causes a negative Hall voltage to appear at the transverse sensors. The peak magnitude of B_z under the edge of F is several kOe and B_z decays to negligible magnitude on a length scale of order 100 nm [6–9]. An external in-plane field H_x used to orient the magnetization \vec{M} causes no Lorentz force on the carriers and does not directly affect the output.

In our prototypes, the high mobility heterostructure is grown by molecular beam epitaxy (MBE) and consists of: 3 nm InAs/25 nm $\text{Al}_{0.6}\text{Ga}_{0.4}\text{Sb}$ (I_1 in Fig. 1C)/15 nm InAs/200 nm $\text{Al}_{0.6}\text{Ga}_{0.4}\text{Sb}$ /3 μm AlSb (I_2 in Fig. 1C)/semi-insulating GaAs (0 0 1) substrate. Doping of the InAs layer was achieved by an arsenic soak in the middle of the 25 nm $\text{Al}_{0.6}\text{Ga}_{0.4}\text{Sb}$ barrier. This technique increases the sheet carrier density in the InAs layer by a factor of 3–4, with the likely source of electrons being As-on-Al antisite defects [10,11]. After a micron-scale Hall cross is fabricated by photolithography and a mesa etch, the F layer is fabricated by photo- or electron beam-lithography and liftoff. The prototype of Fig. 1A demonstrates device scaling with the minimum feature size $f = 500$ nm. The F film was e-beam deposited from a single charge of $\text{Ni}_{0.8}\text{Fe}_{0.2}$ in a vacuum of 10^{-6} Torr to a thickness of 16 nm, and an e-beam lithography was used to pattern the element with dimensions $a = 500$ nm, $b = 2.2$ μm (refer to Fig. 1B). The entire chip was then passivated with an 80 nm thick coating of SiO_2 , and a focussed ion beam was used to narrow the dimensions of the Hall cross by cutting trenches that penetrated the InAs layer (Fig. 1A), leaving a cross with arm width $c = 700$ nm.

The bipolar Hall output voltage is linear with bias current for the experimental range of 50 μA to 2 mA and is given by $V_H/I = \pm\Delta R_H$ for the bistable states $\pm\vec{M}$. A small geometric asymmetry in the fabrication of the

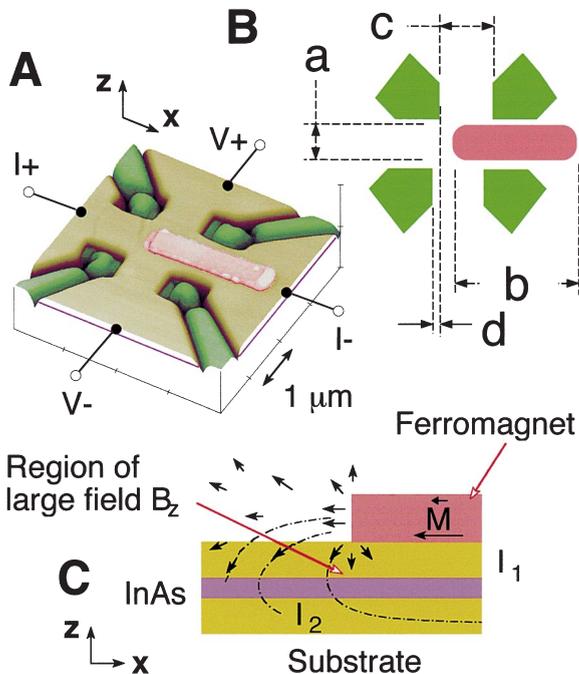


Fig. 1. Ferromagnet–semiconductor nonvolatile gate: (A) AFM false color image – the ferromagnetic element is red, the semiconductor mesa is brown, the buried SQW is purple, and regions made electrically insulating by focussed ion beam irradiation are green. (B) Schematic top view. (C) Cross-section view showing magnetic fringe field \vec{B} generated at edge of F , which has a large component $\pm B_z$ in the vicinity of the SQW (purple).

¹ We adopt the convention that \vec{B} refers to magnetic fields generated by F , \vec{H} refers to externally applied magnetic fields, and we use the units Oe and G interchangeably.

voltage arms, shown as a lithographic offset d in Fig. 1B, adds a small series resistance R' to the sense circuit. In a device with $R' = \Delta R_H$, the LOW and HIGH output states take the convenient values 0 and $2\Delta R_H$, representing “0” and “1”, respectively.

The binary states of a ferromagnetic film are correlated with logical LOW and HIGH input levels by inductively coupling the magnetization to digital electric current pulse in an integrated “write wire.” A micron scale prototype was fabricated in the manner described above, and a thin, patterned Au wire was added as an additional level. In the false color AFM image of Fig. 2, the overlaid Au wire is yellow. When a positive (negative) current I_w flows in the write wire, a positive (negative) magnetic field H_x beneath the wire and parallel to the axis of F orients the magnetization to the left (right) resulting in the binary state “1” (“0”). The magnitude of H_x is directly proportional to the amplitude of current I_w , $H = \alpha I_w$ with α an inductive coupling constant, and is weakly dependent on the distance beneath the wire. In our micron scale prototypes, a current of about 100 mA in a 12 μm wide write wire resulted in a 50 Oe field.

3. Results and discussion

For the prototype of Fig. 2, F was e-beam deposited from a single charge of $\text{Fe}_{0.1}\text{Co}_{0.9}$ in the presence of a growth field of about 200 Oe oriented along \hat{x} . The thickness was $d = 60$ nm, and the rectangular shape with

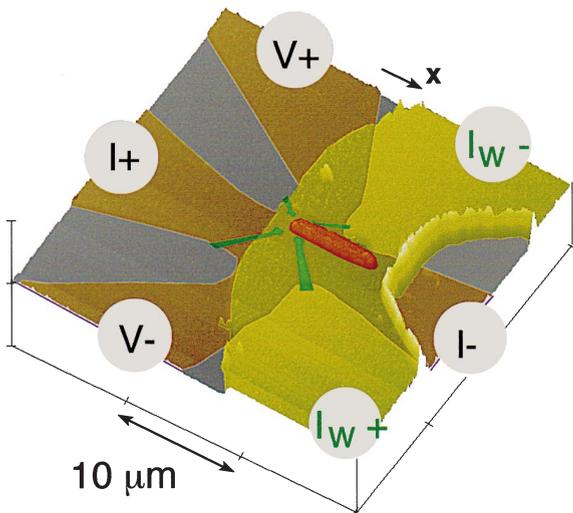


Fig. 2. AFM image of ferromagnet–semiconductor nonvolatile gate with integrated write wire. In this false color image, the ferromagnetic element F is red, the semiconductor mesa is brown, electrically insulating regions of the mesa are dark green, and the write wire is yellow.

transverse dimensions $a = 1.5 \mu\text{m}$, $b = 7.5 \mu\text{m}$ was achieved by optical lithography and liftoff. After processing, Van der Pauw measurements determined that the room temperature carrier density was $1.8 \times 10^{12} \text{ cm}^{-2}$, the mobility was $22,000 \text{ cm}^2 \text{ V}^{-1}\text{s}^{-1}$, and the sheet resistance was $R_{\square} = 150 \Omega/\square$. A small lithographic asymmetry of $b \approx 70$ nm resulted in an offset of $R' = \Delta R_H$. The quasistatic output characteristic, measured with a steady-state bias current and an externally applied field H_x , is shown in Fig. 3A (all data are for room temperature). The coercivity of F is $H_c = 90$ Oe, with full saturation magnetization (zero slope in the $R_H(H)$ loop) achieved at about 200 Oe. The nonvolatile, nonpowered condition is $H_x = 0$, and the bistable device states correspond to the two remanent magnetization states with levels LOW = 0 Ω and HIGH = 8.5 Ω . The

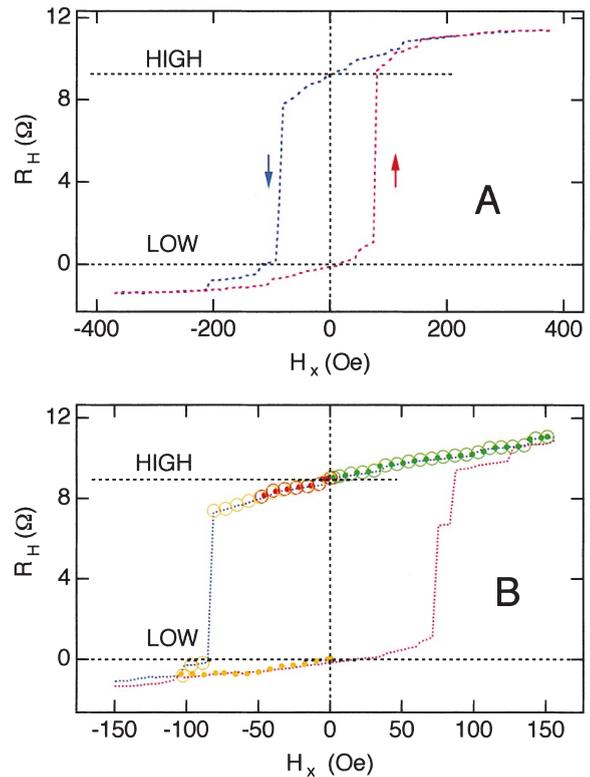


Fig. 3. Quasistatic hysteresis loop, $R_H(H)$, of an integrated device: (A) Full hysteresis loop, as H_x is swept from -380 Oe to $+380$ Oe and back. The two remanent states, $R_H(0)$, are marked HIGH and LOW. (B) Dotted lines, hysteresis loop measured for field sweep from -150 to $+150$ Oe and back (note change of scale from (A)). Symbols: response to the following quasistatic field sweeps. Starting from the HIGH remanent state, open circles represent increasing field magnitude and closed circles represent decreasing magnitude. Green symbols: 0–150 Oe and back. Red symbols: 0 to -50 Oe and back. Yellow symbols: 0 to -100 Oe and back. All data are for room temperature.

difference between LOW and HIGH is slightly less than the full output swing $2\Delta R_H = 12.5 \Omega$.

Further measurements confirmed details of the $R_H(H)$ loop as shown in Fig. 3B (note the change of scale from Fig. 3A). Open circles are used for increasing field magnitude and closed circles for decreasing magnitude. Starting at the HIGH state, when the external field is quasistatically swept to 150 Oe and back to $H_x = 0$ (green symbols) the $R_H(H)$ response reversibly traces the upper portion of the loop and returns to the HIGH state. Similarly, a quasistatic field sweep from $H_x = 0$ to -50 Oe and back (red symbols) results in a reversible trace that returns to HIGH. However, when the field is swept from $H_x = 0$ to -100 Oe and back (yellow symbols), a hysteretic loop is traced and the value of R_H is set to LOW.

As the dynamics of magnetization reversal in microstructured ferromagnetic elements occur on a time scale of ns or less [12], the magnetic manipulations described in Fig. 3 could also be achieved using current pulses applied to the integrated write wire, and then the result is a magnetoelectronic Boolean logic operation. The sketch of Fig. 4A is a schematic representation of the prototype device of Fig. 2. Binary input pulses may

be applied simultaneously to input terminals A and B or to a control terminal C and thereby transmitted down a write wire. A Boolean logic process requires only two clock steps for completion and the result is then latched so it can be read out at any later time. This operation is demonstrated with the data of Fig. 4C using individual pulses. The Hall device is biased with a steady-state dc current (0.1 mA) and the readout voltage is recorded, as current pulses are applied to the input write wire terminal (refer also to Fig. 2).

We begin by following the same sequence of Fig. 3C: a “reset” pulse of amplitude 150 Oe applied to terminal C sets the initial state of the device to HIGH. A pulse of -50 Oe is insufficient to switch the state of the device, and it remains in the HIGH state. After a reset pulse ensures that the initial device state is HIGH, a pulse of -100 Oe ($t = 75$) traverses the hysteresis loop and the device switches to LOW. By identifying a -50 Oe pulse as “unit” write current $-I_w$ associated with the binary “1,” we recognize the above sequence as a demonstration of a Boolean NAND operation, $\overline{A \cdot B}$: A single unit current pulse $-I_w$ (“1”) applied to either terminal A or B is insufficient to switch the device and the state remains HIGH (“1”), but two unit current pulses applied

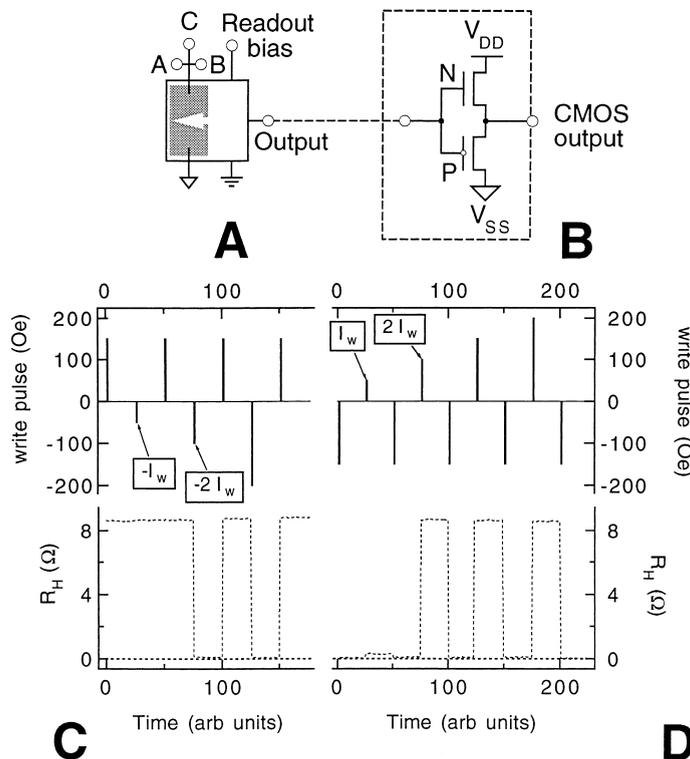


Fig. 4. (A) Schematic representation of integrated device of Fig. 2, with input terminals A–C, and separate terminals for bias and readout. (B) FET components that could be used to make a CMOS compatible cell. (C, D) Steady-state response to input bias pulses that demonstrate: (C) $\overline{A \cdot B}$, $\overline{A + B}$; and (D) $A \cdot B$, $A + B$.

simultaneously to terminals A and B, with net magnitude $-2I_w$, successfully switch the device and the state changes to LOW (“0”).

Continuing the progression, after a reset pulse sets the device state to HIGH ($t = 100$), a -200 Oe pulse ($t = 125$) also traverses the loop and the device switches to LOW. By identifying a -100 Oe pulse as a unit write current $-I_w$, we recognize this to be a demonstration of a Boolean NOR operation, $\overline{A+B}$: A current pulse of unit amplitude I_w applied to either terminal A or B, or to both terminals A and B, changes the device state to LOW (“0”).

The inverse operations AND and OR result by changing the polarity of the input write pulses, as demonstrated in Fig. 4D. After a reset pulse of -150 Oe sets the initial device state LOW (“0”), a single pulse of unit amplitude $\alpha I_w = 50$ Oe fails to change the device state, and it remains LOW (“0”). After another reset pulse ensures the initial device state to be LOW, two simultaneous pulses with net amplitude $2I_w$ ($t = 75$) traverse the hysteresis loop and set the device to HIGH (“1”). This is a Boolean AND operation, $A \cdot B$. Finally, if the unit amplitude is renormalized to $\alpha I_w = 100$ Oe, this step shows that a single pulse I_w applied to either terminal A or B switches the device to HIGH (1). The 200 Oe pulse ($t = 175$) shows that two pulses with net amplitude $2I_w$ also result in setting the device to HIGH (“1”). This is a Boolean OR operation, $A + B$.

Remarkably, this single magnetoelectronic device can perform any of the four Boolean operations in only two clock cycles, and the function to be performed is determined instantaneously by the way the device is addressed: The normalized value of I_w has one of two values and either of two polarities.

An equivalent mode of operation is even simpler. A control pulse applied to terminal C, simultaneously with the input pulses applied to A and B, determines the function of the device. If a zero amplitude pulse is applied to C, unit pulses I_w at A and B are required to switch the device state, and it operates as an AND gate. If a unit amplitude pulse I_w is applied to C, then a single unit pulse at either A or B is necessary and sufficient to switch the device state. The 150 Oe pulse ($t = 125$) in Fig. 4D confirms that simultaneous pulses applied to A–C, with a net write current of $3I_w$, also switches the device state, confirming operation as an OR gate. By changing the polarity of the control pulses at terminal C, the device function can be set to be a NAND or NOR gate. Once again, a single magnetoelectronic device can perform any of four Boolean functions in only two clock cycles, and the function is programmatically controlled, instantaneously, by a single control pulse.

A demonstration of device operation using control pulses is shown with the data of Fig. 5. Each of seven operations begins with a reset pulse at input C. In the next clock cycle, a “0” or “1” control pulse is applied to

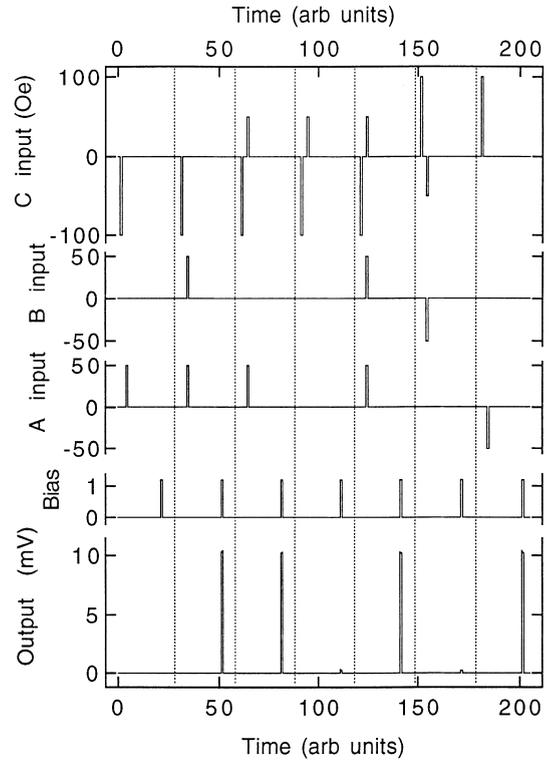


Fig. 5. Demonstration of gate operation using control pulses. In each of the seven operations shown, a reset write pulse is applied to terminal C during the first clock cycle. In the second cycle, a control write pulse is applied to C, input write pulses are applied to A and B, and the result is latched. The output is read out at some later time by applying a read bias pulse to the Hall device and detecting LOW or HIGH voltage levels. In these data, the time delay before readout was varied from a few s to 100 h. “A Input,” “B Input” and “C Input” are in units of Oe, “Bias” is in units of mA.

C and, simultaneously, input values of “0” or “1” are applied to terminals A and B. The result is formed and latched during this second cycle, and can be read out at a later time by applying a bias pulse. Here we use 1.2 mA read bias pulses applied to the Hall device so that the Hall output voltage levels are 0 ± 0.2 mV for LOW and 10.4 ± 0.3 mV for HIGH. The data of Fig. 5 represent these Boolean operations: AND ($A = 1, B = 0$); AND ($A = 1, B = 1$); OR ($A = 1, B = 0$); OR ($A = 0, B = 0$); OR ($A = 1, B = 1$); NOR ($A = 0, B = 1$); and NAND ($A = 1, B = 0$).

We have used a low frequency measuring apparatus and pulses with duration of order 100 μ s. However, magnetization reversal in microstructured ferromagnetic elements occurs on a time scale of a few ns or less [12] so that processing speeds of order 1 GHz can reasonably be expected. Another feature of the ferromagnet–semiconductor nonvolatile gate is *inverse scalability*: device

characteristics improve as the device dimension shrinks. The micron scale prototype of Fig. 2 (with F dimensions 1.5 μm by 7.5 μm) had a coercivity of 90 Oe, and a current pulse of magnitude 100 mA in a 12 μm wide write wire corresponded to $\alpha I_w = 50$ Oe. A prototype device with dimensions 500 nm in width and 2.2 μm in length and with comparable output characteristics had a coercivity of 50 Oe. A current pulse with amplitude 12 mA in a 2.5 μm wide write wire would correspond to $\alpha I_w = 25$ Oe. For a metallized write wire with resistance $R \approx 1 \Omega$, the power consumption of this device would be the order of 0.1 mW for both writing and reading (assuming 1 mA bias and a device impedance of $R_{\square} \sim 100 \Omega$), and the quiescent power would be zero.

Like the RTD, the ferromagnet–semiconductor nonvolatile gate does not presently have enough gain for fanout (i.e. the ability to drive subsequent devices linked in a chain). However, the device has shown voltage output levels of order 0.1 V [6–9], adequate for integration with transistor based devices. For example, the design of the fully restored CMOS logic family uses n-channel and p-channel FETs at the output stage of each Boolean gate to set the output LOW and HIGH voltage levels to V_{SS} and V_{DD} , respectively. Similarly, the magnetoelectronic Boolean gate of Fig. 4A can be combined with a pair of FETs (Fig. 4B) to yield a cell with the flexibility of continuously dynamic addressability and with fully restored CMOS output levels.²

While we have demonstrated the four basic Boolean operations, other functions are readily accomplished. For example, the exclusive OR (XOR) operation can be performed with two magnetoelectronic gates in series, with the output of one driving the read bias of the second. Unlike the RTD which has narrow margins for input voltages, an appropriately chosen value of input current I_w could tolerate a large variation, $\pm 20\%$.

The data of Fig. 5 also demonstrate the write and read operations of a magnetoelectronic nonvolatile memory cell. A recent nonvolatile storage cell based on a ferroelectric device [14] has comparable readout discrimination, but suffers a retention loss of a few percent per hour. Our ferromagnet–semiconductor nonvolatile gate devices have shown no measurable retention loss after 100 h. A typical storage cell prototype has area $18f^2$ and essentially uses the same design as the addressable Boolean gate. Thus, the prospect exists for fabricating high density arrays of high speed devices, with a particular logic or storage function determined dynamically and programmatically for each device.

4. Summary

We have introduced a magnetoelectronic device “family” composed of a single device that can perform any of several Boolean functions, with the function dynamically determined *during the operation* by the manner in which the device is addressed. The device also performs a nonvolatile storage function so that integration of logic and memory (on chip) is automatically achieved. With an array of devices, memory and processing functions could be dynamically apportioned.

Acknowledgements

This work was supported by the Office of Naval Research (ONR) and the Defense Advanced Research Projects Agency (DARPA). The authors are grateful to S. Bounnak, M.J. Yang, and R. Bass for technical assistance. M.J. gratefully acknowledges the stimulating conversations with J.N. Gross.

References

- [1] Turton R. The quantum dot. New York: Oxford Univ Press, 1996 [chapter 9].
- [2] Simonds JL. *Physics Today* 1995;48(4):26.
- [3] Prinz GA. *Science* 1998;282:1660.
- [4] Tehrani S, Chen E, Durlam M, DeHerrera M, Slaughter JM, Shi J, Kerszykowski G. *J Appl Phys* 1999;85:5822.
- [5] Johnson M. *Science* 1993;260:320.
- [6] Johnson M, Bennett BR, Yang MJ, Miller MM, Shanabrook BV. *Appl Phys Lett* 1997;71:974.
- [7] Reijniers J, Peeters FM. *Appl Phys Lett* 1998;73:357.
- [8] Geim AK, Dubonos SV, Lok JGS, Grigorieva IV, Maan JC, Hansen LT, Lindelof PE. *Appl Phys Lett* 1997;71:2379.
- [9] Monzon FG, Johnson M, Roukes ML. *Appl Phys Lett* 1997;71:3087.
- [10] Tuttle G, Kroemer H, English JH. *J Appl Phys* 1990; 67:3032.
- [11] Bennett BR, Shanabrook BV. Molecular beam epitaxy of Sb-based semiconductors. In: Liu WK, Santos M, editors. *Heteroepitaxy: thin film systems*. Singapore: World Scientific, 1999. p. 401–52.
- [12] Freeman MR, Hiebert WK, Stankiewicz A. *J Appl Phys* 1998;83:6217.
- [13] Villasenor J, Mangione-Smith WH. *Sci Am* 1997;276:66.
- [14] Mathews S, Ramesh R, Venkatesan T, Benedetto J. *Science* 1997;276:238.

² The conventional approach to “field programmable logic” involves high level blocks of hard-wired devices and “programming” times of order 1 ms to 1s (see e.g. Ref. [13]).