# Current collapse induced in AlGaN/GaN high-electron-mobility transistors by bias stress

J. A. Mittereder,[a)] S. C. Binari, P. B. Klein, J. A. Roussos, D. S. Katzer, D. F. Storm, D. D. Koleske,[b)] A. E. Wickenden,[c)] and R. L. Henry
*Naval Research Laboratory, Washington D.C. 20375*

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Current collapse is observed to be induced in AlGaN/GaN high-electron-mobility transistors as a result of short-term bias stress. This effect was seen in devices grown by both metalorganic chemical vapor deposition (MOCVD) and molecular-beam epitaxy (MBE). The induced collapse appears to be permanent and can be reversed by SiN passivation. The traps responsible for the collapse have been studied by photoionization spectroscopy. For the MOCVD-grown devices, the same traps cause the collapse in both unstressed and stressed devices. These effects are thought to result from hot-carrier damage during stress. [DOI: 10.1063/1.1604472]

Gallium nitride high-electron-mobility transistors (HEMTs) have recently received significant attention because of their potential for use in high-power solid-state microwave applications. While very high output power densities have been demonstrated, significant developmental work remains for GaN HEMTs to become viable. One of the key remaining issues is that of device reliability, and it has been reported that the output power from these devices can permanently degrade, to varying degrees, over relatively short periods of time (e.g., 10 h).[1–3] In this work, we have studied an important mode of degradation that has not been previously recognized in nitride devices. We observe that current collapse can be induced in the device–drain characteristics as a result of short-term (several hours) dc bias stress. The term ''current collapse'' is taken here as the reduction in dc drain current after the application of a high drain–source voltage.[2] The high voltage leads to the injection of hot carriers into regions of the device adjacent to the conducting channel that contain deep traps. The trapping of these hot carriers leads to a reduction in the drain current that persists as long as the carriers remain trapped. We have observed that current collapse can be induced in devices that exhibit no collapse by exposing the device to a high voltage over a long period of time (i.e., stress). Because of the origins of current collapse, the affect of the stress must be to introduce deep levels into the structure. Current collapse reduces the maximum available drain current and increases the knee voltage, thereby limiting the drain current and voltage excursions and resulting in a reduced microwave output power. Thus, induced current collapse can be a significant factor in the observed degradation of HEMT output power. We have observed stress-induced collapse in AlGaN/GaN HEMTs fabricated from epitaxial layers grown both by molecular-beam epitaxy (MBE) and by metalorganic chemical vapor deposition (MOCVD).

Devices fabricated from fifteen MBE-grown structures and from four MOCVD-grown structures were evaluated. The MBE structures consisted of a 0.1-$\mu$m-thick AlN buffer layer, a 1-$\mu$m-thick undoped GaN buffer/channel layer, and an undoped 250-Å-thick $Al_{0.25}Ga_{0.75}N$ barrier layer. These layers were grown on either $n^+$-6H-SiC or semi-insulating 4H–SiC using procedures similar to those reported previously.[4] The sheet resistance, $R_{sh}$, of most of these layers was in the range of 500 to 650 Ω/□, while five wafers had a sheet resistance over 700 Ω/□. This large variation in $R_{sh}$ is a result of these wafers being part of an MBE-growth development effort, but it was determined that $R_{sh}$ was not correlated with the induced current collapse. The MOCVD structures were grown from two reactors on sapphire substrates using parameters previously reported[5] and consisted of a 200 Å low-temperature AlN nucleation layer, a 3-$\mu$m-thick undoped GaN buffer/channel layer, and an undoped 250-Å-thick $Al_{0.30}Ga_{0.70}N$ barrier layer. The $R_{sh}$ of the MOCVD layers was between 350 and 600 Ω/□.

HEMTs were fabricated with source–drain spacings of 3 to 6 $\mu$m, gate lengths of 0.5 to 1.5 $\mu$m, and widths of 150 $\mu$m. Ohmic contacts were formed by rapid thermal annealing using either Ti/Al alloyed at 600 °C or Ti/Al/Ni/Au alloyed at 900 °C. Both Ni/Au and Pt/Au were utilized for the gate metallization. Either implant isolation or reactive ion etching mesa etching techniques were used for device isolation. These variations in ohmic, mesa, and gate processing are not correlated with the induced current collapse. Some of the HEMTs considered in this study were passivated with 1000 Å of plasma-enhanced chemical vapor deposition silicon nitride. For these cases, the nitride passivation was deposited after the ohmic alloy, device isolation, and gate metal deposition processing steps were completed.

A microwave probe station was used for the stress tests to ensure stable electrical contact during the test. A computer-controlled Agilent 4142B Modular dc Source/Monitor (Agilent, Palo Alto, CA) was used for all of the bias stressing and current–voltage measurements. The bias stress consisted of maintaining the device at a fixed drain–source voltage ($V_{DS}$) and fixed gate–source voltage ($V_{GS}$) for periods of 4 to 100 h. The devices were measured and stressed in the dark to avoid possible influence from the laboratory lighting. Prior to measurement, the stressed devices were ex-

a)Electronic mail: mittereder@estd.nrl.navy.mil
b)Present address: Sandia National Laboratories, Albuquerque, NM 87185.
c)Present address: U.S. Army Research Laboratory, Adelphi, MD 20783.

 

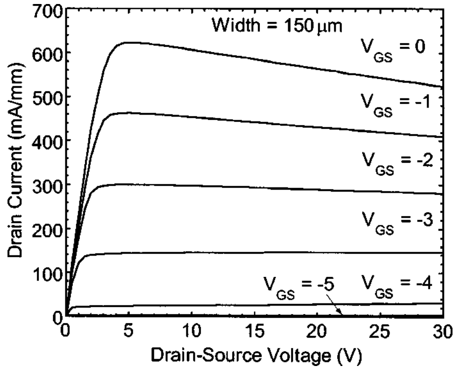


FIG. 1. Drain characteristics of a representative unstressed GaN MBE HEMT exhibiting no current collapse.

posed to UV light to detrap electrons that may have been trapped during the bias stress. In order to study the nature of the traps causing the collapse, photoionization spectroscopy (PS) measurements were carried out using a xenon lamp and a 0.22 m double spectrometer as a tunable light source. Experimental details of this measurement are described in Ref. 6.

The current–voltage (I-V) characteristics of a typical unpassivated MBE device before stress are shown in Fig. 1. No evidence of current collapse is apparent, as was the case for all of the MBE-grown HEMTs. The MBE devices were bias stressed at a $V_{DS}$ of 30 V, and $V_{GS}$ was set to give an initial drain current density of 200 mA/mm. Substantial current collapse was observed which was induced after stress for many of the devices. This effect is illustrated in Fig. 2. For the purpose of clarity, a single value of $V_{GS}=0$ V was used for this measurement. The main part of Fig. 2 shows two sets of data, each set consisting of three consecutive $V_{DS}$ sweeps (labeled 1, 2, and 3) taken within a 10-s-time period. The first set (dashed lines in Fig. 2) was taken before stress was applied. After the first sweep is completed and a high voltage has therefore been applied to the drain, only a small reduction in drain current is observed in the second and third sweeps (coincident), indicating only a small amount of current collapse. The second data set (solid lines in Fig. 2) was taken after the device was stressed for 16 h. The second and third sweeps of this set (almost coincident) exhibit a large reduction in drain current relative to the first, indicating significant collapse. To characterize the degree of collapse

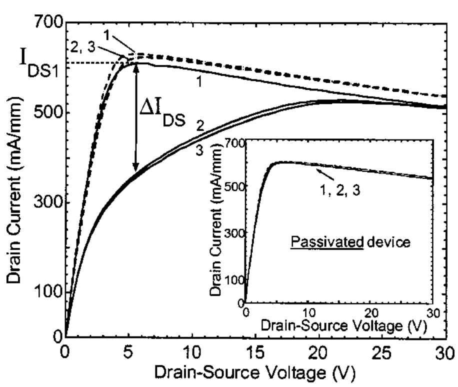


FIG. 2. Current collapse is induced after stressing an unpassivated GaN MBE HEMT (dashed lines: Before stress; solid lines: After stress). Inset: Drain characteristics of a similar device that was stressed after passivation.

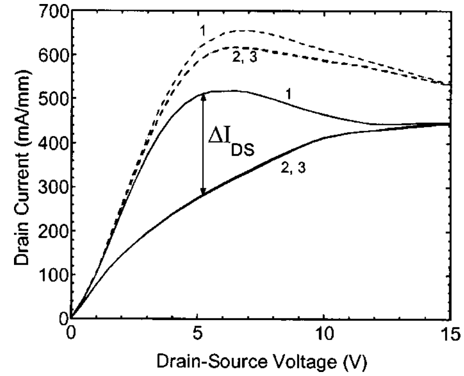


FIG. 3. Drain characteristics exhibiting current collapse due to stress in an unpassivated GaN MOCVD HEMT (dashed lines: Before stress; solid lines: After stress).

quantitatively, we define a normalized current collapse parameter, $\Delta I \equiv \Delta I_{DS}/I_{DS1}$, where $\Delta I_{DS}$ is the observed reduction in drain current below that of the first $V_{DS}$ sweep, measured at the $V_{DS}$ where this reduction is a maximum. $I_{DS1}$ is the corresponding drain current of the first sweep at this same $V_{DS}$ (see Fig. 2). A significant variation in $\Delta I$ was observed between the 15 MBE-grown wafers that were evaluated. For a 16-hour-long bias stress, $\Delta I$ varied between 0.01 and 0.41. The magnitude of the induced current collapse, and thus the rate at which empty deep traps were introduced, was observed to increase with stress time, stress–drain voltage, and stress drain current. The induced current collapse appears to be permanent, as it was found to persist for months after the stress. The induced deep traps are apparently relatively stable.

For the MOCVD devices, a lower drain voltage was used because of the lower thermal conductivity of the sapphire substrate. All of the MOCVD wafers tested showed some current collapse before stress ($\Delta I \sim 0.06$ to 0.24), as they already contained a substantial concentration of deep traps. An additional induced collapse ($\Delta I = 0.31$ to 0.48) was observed after stressing for 16 h. This is shown in Fig. 3 for a 150 $\mu$m device that was stressed at $V_{DS}=15$ V with $V_{GS}$ set to give an initial drain current density of 200 mA/mm.

In order to probe the nature of the defects responsible for the induced collapse, several MBE devices were stressed after the deposition of a silicon nitride-passivation layer. Shown in the inset of Fig. 2 are the characteristics for a SiN-passivated, MBE-grown device that had been bias stressed for 16 h. Minimal, if any, current collapse has been induced in the passivated device using the same stress conditions (16 h, $V_{DS}=30$ V, and $I_{DS}=200$ mA/mm) as the device shown in the main part of Fig. 2. Prior to passivation, neighboring devices from this wafer consistently showed current collapse after stress, similar to that shown in Fig. 2. However, longer-term stress at higher drain current (64 h, $V_{DS}=30$ V, and $I_{DS}=540$ mA/mm) did lead to the emergence of some collapse ($\Delta I = 0.13$) for this passivated device. Thus, passivation appears to inhibit current collapse from being induced by bias stress, but does not prevent it completely.

In addition to inhibiting the stress-induced current collapse as described herein, we have also observed that stress-induced collapse can be fully or partially reversed by depositing a SiN layer *after* the stress. For unpassivated devices that displayed a moderate amount of induced collapse (i.e. $\Delta I \sim 0.15$), the stress-induced collapse can be fully reversed by SiN passivation, while devices with higher values of induced collapse ($\Delta I \sim 0.32$) showed only partial reversal.

Passivation effects, such as those described herein, are often interpreted in terms of surface effects. However, it should be kept in mind that the SiN plasma-enhanced chemical vapor deposition process, which utilizes $SiH_4$ and $NH_3$, exposes the wafer to a high concentration of hydrogen. Therefore, it is possible for hydrogen to diffuse into the device structure where the traps causing current collapse can be passivated by forming H-defect complexes. Hierro *et al.*[7] have shown, for example, that deep defects in GaN can be effectively passivated by exposure to hydrogen. Since some of the traps involved in the collapse have been associated with the GaN buffer layer,[6] it would appear that the reversal of collapse by SiN passivation can occur through H diffusion and subsequent passivation of the deep traps causing the collapse. Hydrogen passivation may also explain the fact that a few (5 out of 15) unpassivated MBE wafers did not exhibit any collapse after stress. This may be due to subtle differences in processing, resulting in a variable exposure to hydrogen that leads to passivation of deep traps in some cases but not in others.[8]

Since current collapse results from an equilibrium concentration of empty deep traps, its appearance as the result of stress must indicate either: (1) the applied stress directly generates the traps,[9] similar to hot-carrier induced defects reported for AlGaAs/InGaAs HEMTs,[10] or (2) pre-existing traps that were inactive (i.e., filled) are activated (i.e., emptied) by the stress due to a hot-carrier-induced shift of the Fermi level. In order to gain further insight into the traps involved in the stress-induced collapse and the mechanism responsible, PS measurements were carried out on devices exhibiting little or no collapse before stress and significant collapse afterward. PS measures the absorption spectrum of the trapped carriers as they are optically released from the traps responsible for the collapse. Previous PS measururements[11] on nonstressed MOCVD nitride-based metal–semiconductor field effect transistors and HEMTs determined that collapse was associated with two trapping centers in the GaN buffer layer—a midgap trap (trap 1) that was thought to be related to structural defects, and a very deep trap (trap 2) that has been associated with the presence of carbon.[12]

The PS spectra of stress-induced collapse in the MOCVD devices reveal only the same two traps as observed in the nonstressed case. Therefore, it is likely that the preexisting traps have been activated, as noted herein. In stressed MBE devices, trap 1 is observed but not trap 2. This is consistent with the smaller concentration of background carbon impurities expected in MBE material. Since trap 1 has been associated with the GaN buffer layer, its appearance in the PS spectra of the MBE devices suggests that it may have the same origin as trap 1 in the MOCVD devices.

In addition, the stress-induced PS spectra in the MBE devices exhibit an absorption threshold near 3.7 eV, which, because of its spectral position, is assumed to be associated with the AlGaN layer. We believe that this feature reflects the photoionization of carriers from ionized shallow acceptors, rather than a deep center that can cause collapse.

In summary, we have observed current collapse induced in MOCVD- and MBE-grown GaN HEMT structures by short-term bias stress. This represents a potential reliability issue for this technology. This effect can be fully or partially reversed by SiN passivation, and it is believed that this results from the diffusion of hydrogen into the device structure, where the responsible deep defects are passivated.

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